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An Investigation into the Effect of the Gate Drive Resistance on the Performance of the Balanced Inverter

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Outline

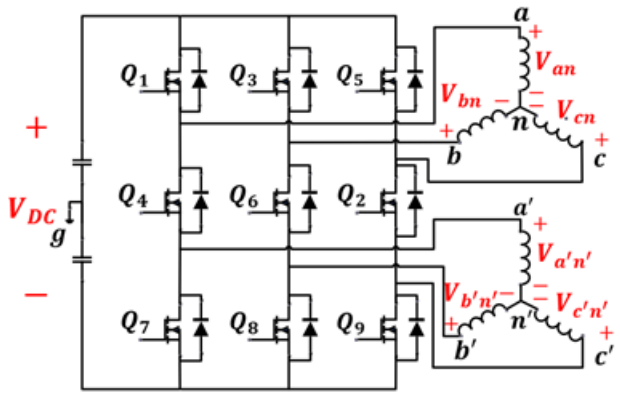
- Introduction
- Switching Event Analysis
- Spectrum of Source CM Voltage
- Experimental Results
- Conclusion

Objectives

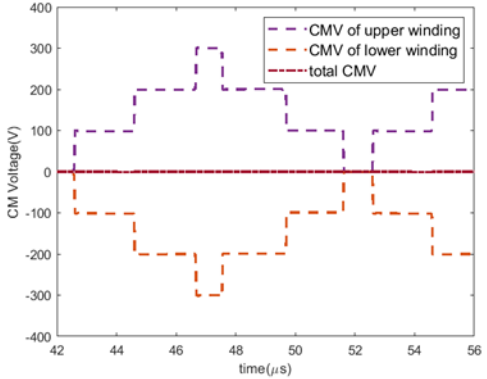
- *Investigate impact of gate resistance on CM EMI performance of balanced inverter*
- *Analyze the switching transient of balanced inverter*
- *Develop a simplified analytical model for predicting impact of gate resistance*
- *Compare source CM voltage of balanced inverter at different gate resistance*
- *Compare the experimental results with analytical predictions*

Introduction to Balanced Inverter

Power Circuit Topology of Balanced Voltage-Source Inverter



CMV of Balanced Inverter Under ideal condition



CMV of balanced inverter is zero theoretically

- Compared with traditional CM EMI suppression solutions such as CM filters, balanced voltage-source inverter can reduce the ***volume***, ***weight***, and ***cost*** of drive system

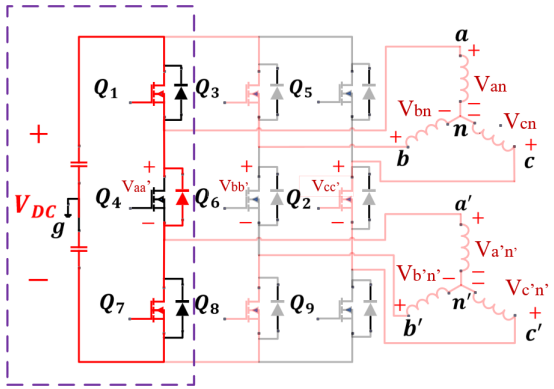
- Although balanced inverter has many benefits, performance of balanced inverter suffers from impact of ***non-ideal*** operation of its hardware implementation such as ***non-symmetrical PCB layout***
- Some efforts have been devoted to investigate impacts of non-ideal operation conditions. However, impact of ***gate drive resistance*** on balanced inverter's performance has ***not*** been investigated
- Existing research concerning impact of gate drive resistance on inverters ***cannot*** be directly applied to balanced inverter
- This paper presents a ***simplified analytical model*** predicting ***impact of the gate drive resistance*** combined with ***unsymmetrical parasitic inductances*** on CM-EMI performance of ***balanced inverter***.

Balanced inverter is a novel solution to CM EMI with significant reduction in volume, weight, and cost of drive system

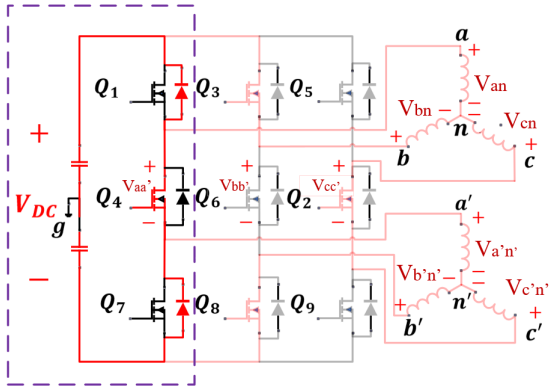
There is a knowledge gap regarding impact of gate drive resistance on performance of balanced inverter

Switching Events Analysis

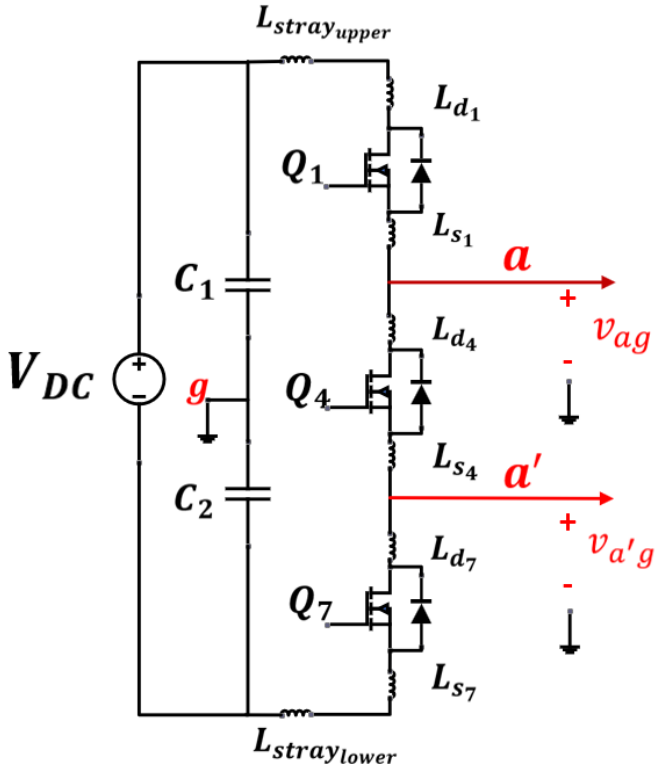
Current flowing into upper winding



Current flowing out of upper winding

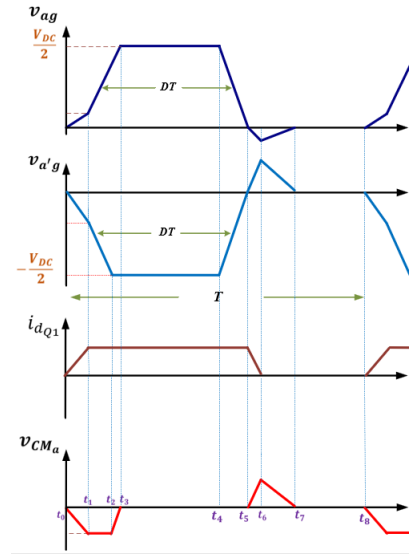


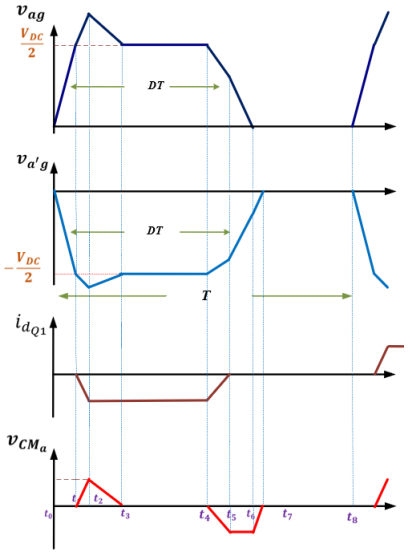
Model of phase A of balanced inverter including parasitic inductances



Upper Winding

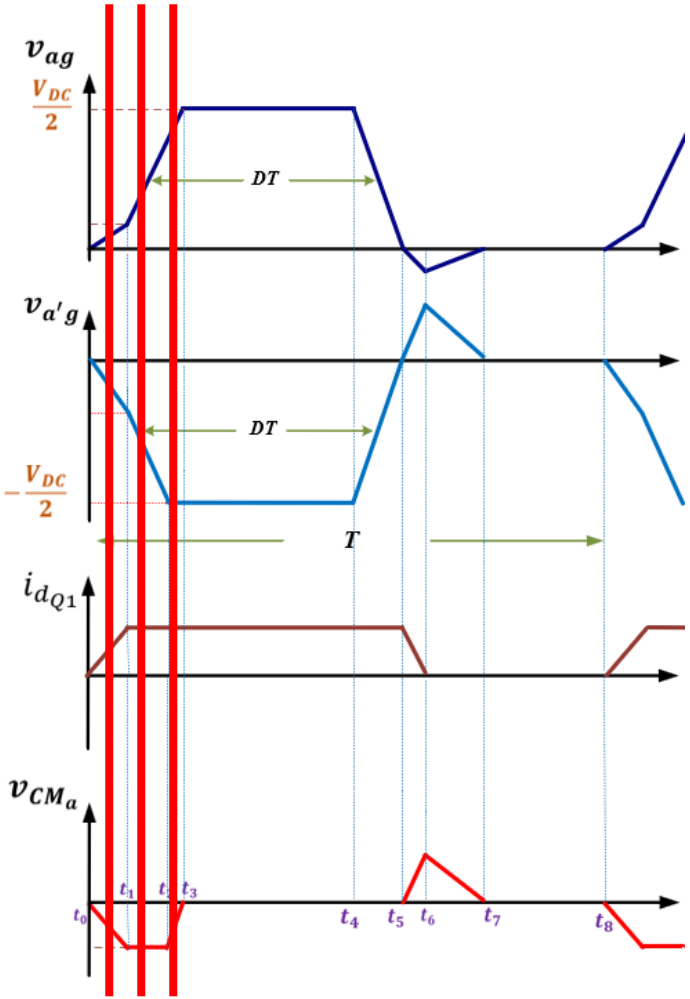
Lower Winding



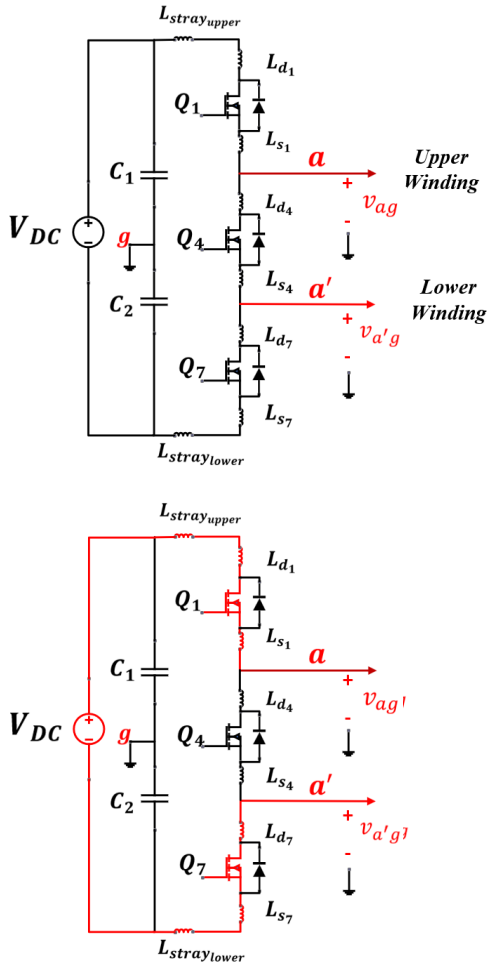


CMV waveform is not affected by the current conduction direction

Turn-on Transient



Model of phase A of balanced inverter incl. parasitic inductances



Period 1 $(t_0 < t < t_1)$

- $i_{d_{Q1}}$ starts to increase
- Due to imbalanced parasitic inductance distribution, Common Mode Voltage generates
- $v_{CM_a} = \frac{v_{ag}+v_{a'g}}{2} = -\frac{L_{difference}a_R}{2t_{ir}}(t-t_0)$

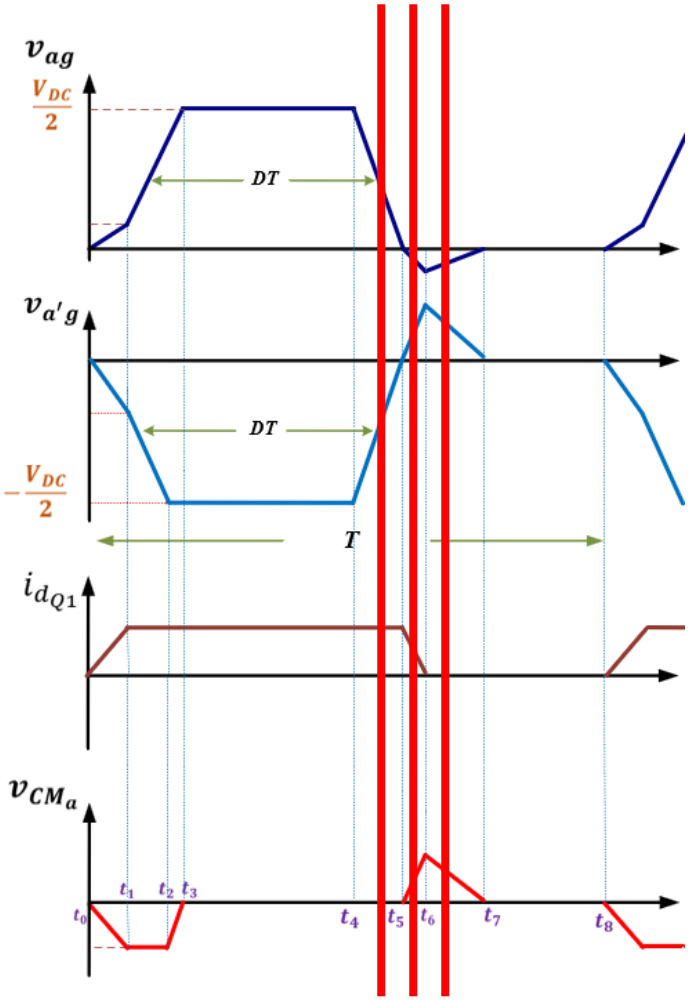
Period 2 $(t_1 < t < t_2)$

- $i_{d_{Q1}}$ reaches target value
- v_{cm} keeps constant

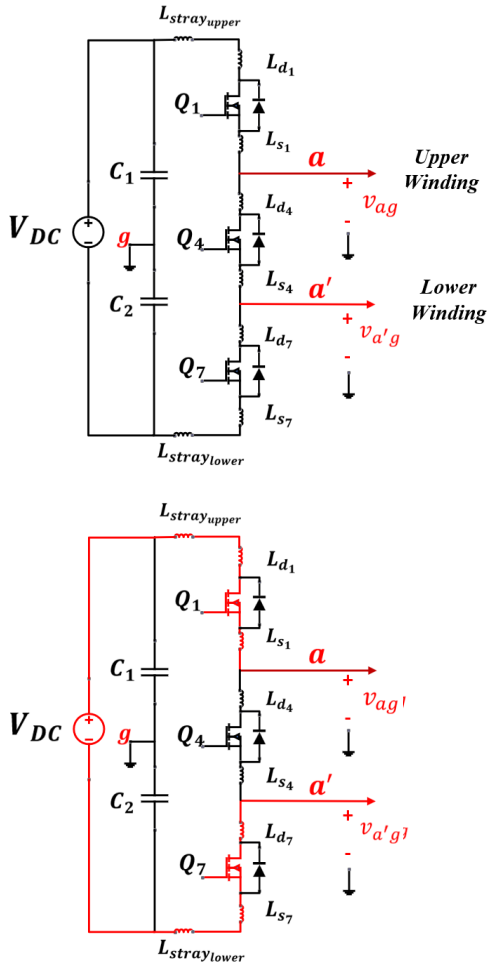
Period 3 $(t_2 < t < t_3)$

- v_{cm} starts to decrease
- $V_{CM_a} = -\frac{L_{difference}a_R}{2} + \frac{b_R}{2}(t-t_{ir}-t_{on})$

Turn-off Transient



Model of phase A of balanced inverter incl. parasitic inductances



Period 4 $(t_4 < t < t_5)$

- Output voltage starts to decrease
- Q_1 and Q_7 still conduct
- $v_{CM_a} = 0$

Period 5 $(t_5 < t < t_6)$

- $i_{d_{Q1}}$ starts to decrease
- $v_{cm} = \frac{L_{difference} d_R}{t_{if}} (\mathrm{t} - t_5)$

Period 6 $(t_6 < t < t_7)$

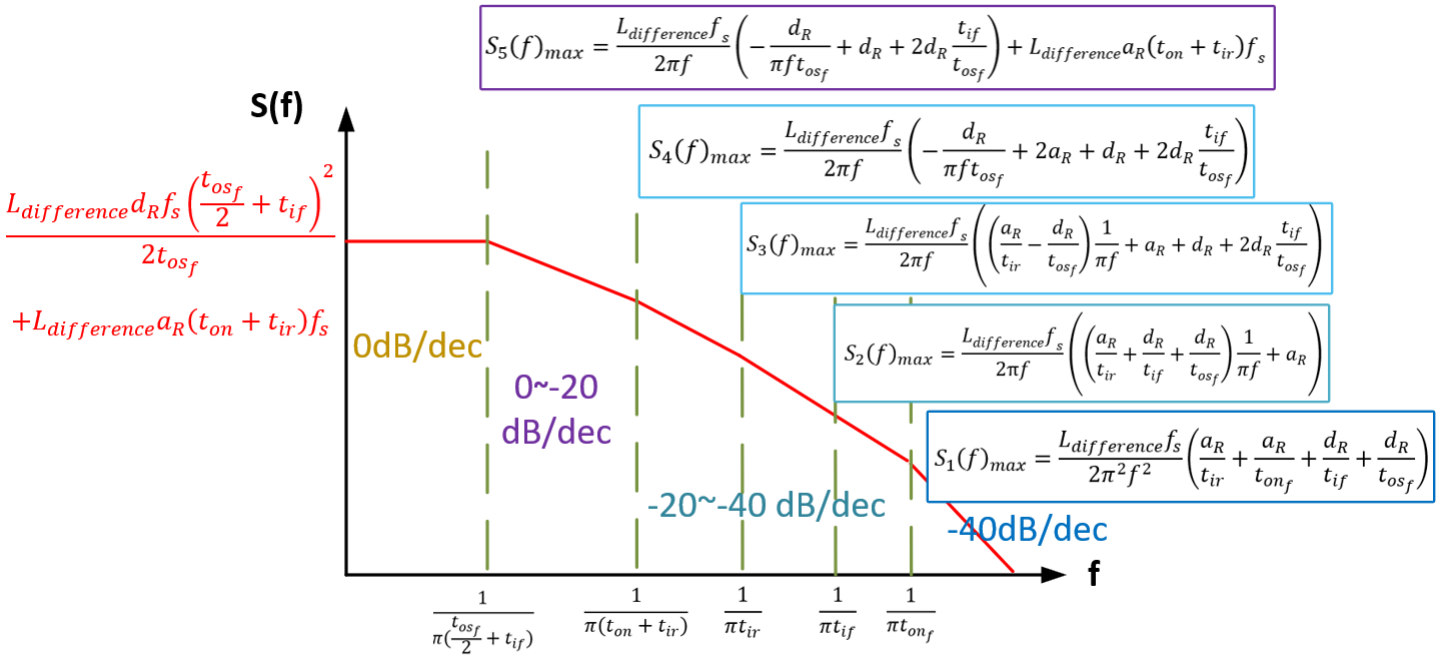
- v_{cm} starts to decrease
- Length of this period is determined by parasitic inductances of power loop and ac parasitic resistance

Spectrum Analysis of Source CM Voltage

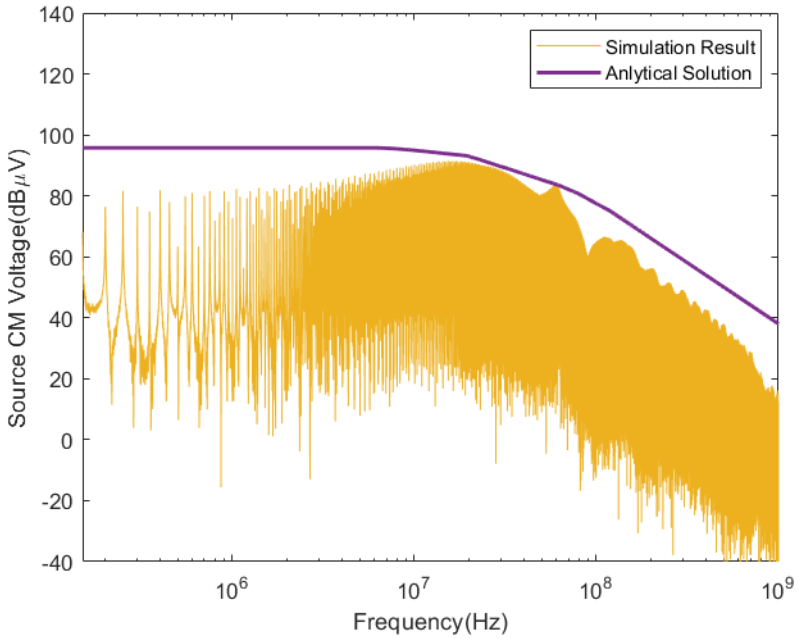
Spectrum of CMV of single phase with fixed duty cycle

$$S(n)=\frac{|L_{difference}|a_R d_R T}{4n^2\pi^2}\left|\frac{1}{d_R}\left[\begin{array}{l}\frac{1}{t_{ir}}\left(1-e^{-j2n\pi t_{ir}/T}\right)+\\ \frac{1}{t_{on_f}}e^{-j2n\pi(t_{on}+t_{ir})/T}\left(e^{-j2\pi n t_{on_f}/T}-1\right)\end{array}\right]-\frac{1}{a_R}\left[\begin{array}{l}\frac{1}{t_{if}}\left(1-e^{-j2n\pi t_{if}/T}\right)+\\ \frac{1}{t_{os_f}}e^{-\frac{j2n\pi t_{if}}{T}}\left(e^{-j2n\pi t_{os_f}/T}-1\right)\end{array}\right]e^{-jn\pi\left(2DT+t_{ir}+t_{on}+t_{off}\right)/T}\right|$$

Analytical approximation of the spectral envelope



Spectrum comparison between simulation and analytical predictions for D=0.3



Spectrum Analysis of Source CM Voltage

Spectrum of CMV of single phase with varying duty cycle(SPWM)

$$S(k)=\frac{|L_{difference}|a_R d_R T}{4k^2\pi^2}\left|\frac{1}{d_R}\left[\frac{1}{t_{ir}}\left(1-e^{-j2k\pi t_{ir}/T}\right)+\frac{1}{t_{on_f}}e^{-j2k\pi(t_{on}+t_{ir})/T}\left(e^{-j2k\pi t_{on_f}/T}-1\right)\right]-\frac{1}{a_R}\left[\frac{1}{t_{if}}\left(1-e^{-j2k\pi t_{if}/T}\right)+\frac{1}{t_{os_f}}e^{-j2k\pi t_{if}/T}\left(e^{-j2k\pi t_{os_f}/T}-1\right)\right]e^{-jk\pi/T\left(T+t_{ir}+t_{on}+t_{off_f}\right)}\sum_{i=0}^{\alpha-1}e^{-jk\pi\, M_0\sin\frac{2\pi i}{\alpha}}/\alpha\right|$$

Spectrum of CMV of three phase with varying duty cycle

$$S_{tot}(k)=\frac{1}{3}\left(S_A(k)+S_B(k)+S_C(k)\right)$$

$$\gamma_a=\frac{\sum_{i=0}^{\alpha-1}e^{-jkn\pi M_0\sin\left(\frac{2\pi i}{\alpha}\right)}}{\alpha}$$

$$\gamma_b=\frac{\sum_{i=0}^{\alpha-1}e^{-jkn\pi M_0\sin\left(\frac{2\pi i}{\alpha}-\frac{2}{3}\pi\right)}}{\alpha}$$

$$\gamma_c=\frac{\sum_{i=0}^{\alpha-1}e^{-jkn\pi M_0\sin\left(\frac{2\pi i}{\alpha}+\frac{2}{3}\pi\right)}}{\alpha}$$

$$S_{tot}(k)=\frac{|L_{difference}|a_R d_R T}{4k^2\pi^2}\left|\frac{1}{d_R}\left[\frac{1}{t_{ir}}\left(1-e^{-j2k\pi t_{ir}/T}\right)+\frac{1}{t_{on_f}}e^{-j2k\pi(t_{on}+t_{ir})/T}\left(e^{-j2k\pi t_{on_f}/T}-1\right)\right]-\frac{1}{a_R}\left[\frac{1}{t_{if}}\left(1-e^{-j2k\pi t_{if}/T}\right)+\frac{1}{t_{os_f}}e^{-j2k\pi t_{if}/T}\left(e^{-j2k\pi t_{os_f}/T}-1\right)\right]e^{-jk\pi/T\left(T+t_{ir}+t_{on}+t_{off_f}\right)}\frac{\gamma_a+\gamma_b+\gamma_c}{3}\right|$$

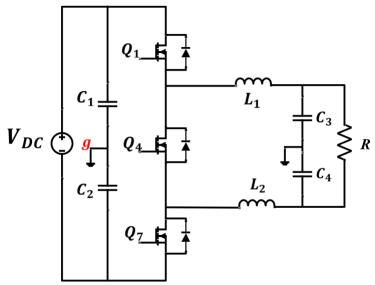
$$\gamma_a=\gamma_b=\gamma_c$$

$$S_{tot}(k)=S_A(k)=S_B(k)=S_C(k)$$

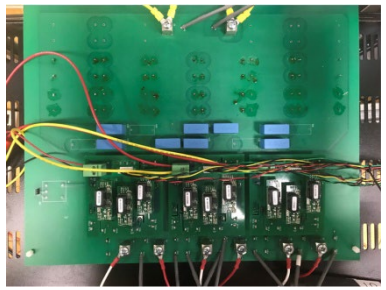
Spectrum envelop for three phase with varying duty cycle is same as that of single phase

Single Phase Test with Fixed Duty Cycle

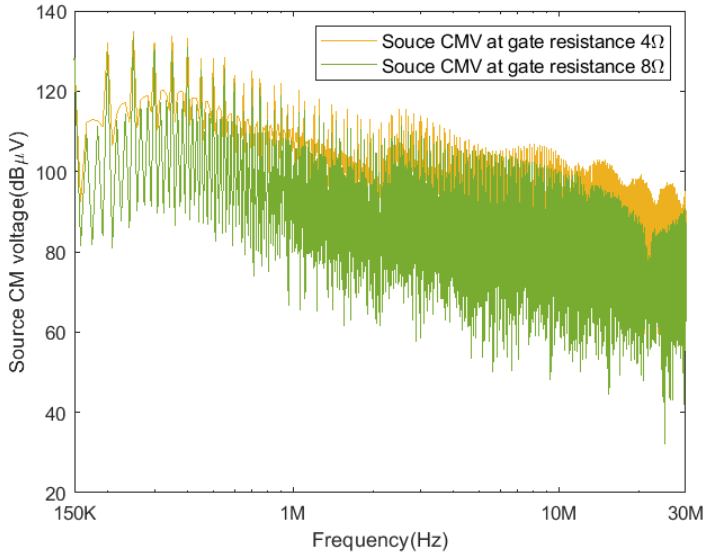
Test circuit for single phase test



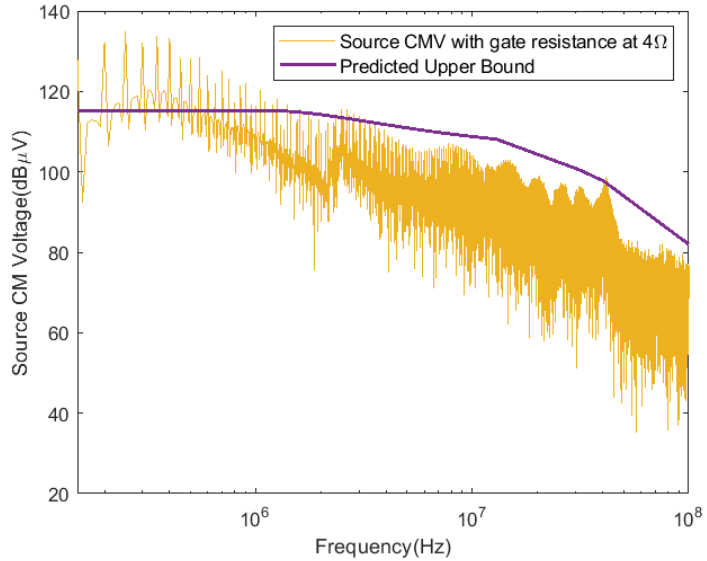
Balanced inverter under test



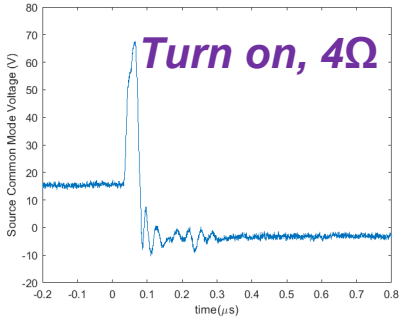
CMV Spectrum Comparison between different gate resistance

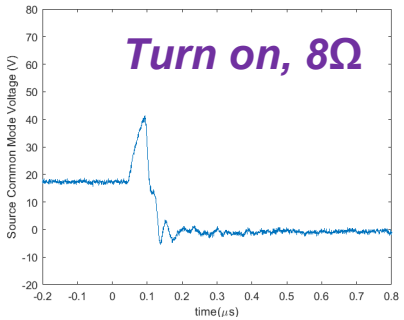


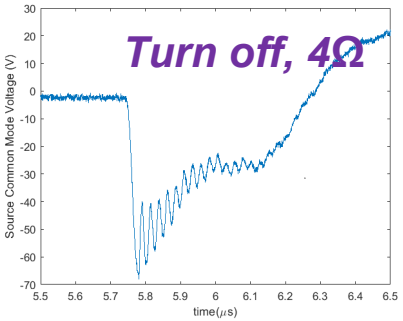
Spectrum comparison between experimental result and analytical predictions

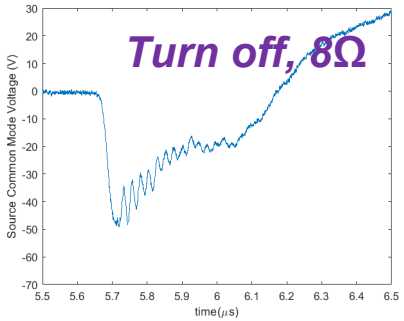


Measure source CM voltage









Measured source CM voltage waveforms match with key features of modeled source CM voltage waveform

When gate drive resistance increases from 4 Ω to 8 Ω, the peak value of CM spectrum decreases by approx. 6 dBμV

Conclusion

- This paper presented a *simplified analytical model* that makes it possible to predict the impact of the gate drive resistance combined with unsymmetrical parasitic inductances on the *CM-EMI* performance of the balanced inverter
- After analyzing the switching events of the balanced inverter, the waveform of the source CM voltage has been investigated in detail considering gate resistance changes and unsymmetrical distribution of parasitic inductance between the upper and lower switches
- Analytical solution of the spectrum of the source CM voltage has been derived, and analytical solution match with the simulation result.
- Experiments have been conducted on an assembled demonstrator version of balanced inverter, and the test results match key features of the modeled source CM voltage waveform. When the gate drive resistance increases from 4 Ω to 8 Ω, the peak value of the spectrum of the source CM voltage decreases by approx. *6 dBµV*, and the estimated efficiency of the power converter decreases from *98.9%* to *98.3%*.
- CM EMI performance of balanced voltage-source inverter is influenced by gate resistance due to the combined effects of changes in the current switching speeds during the switching transients and parasitic inductance differences in the upper and lower inverter halves.

Reference

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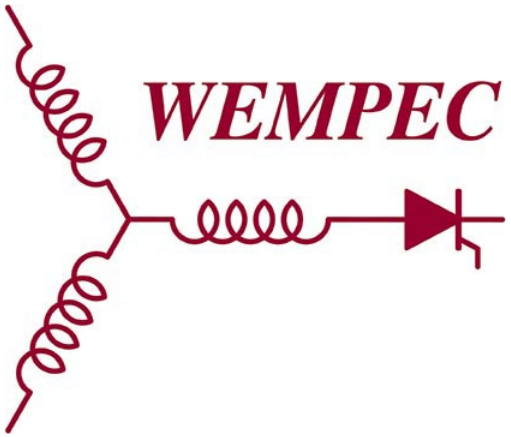
Acknowledgement



Thank You !

Q & A